Operating Requirements

for Altera Devices

January 1998, ver. 8 Data Sheet

Introduction

Altera devices combine unique programmable logic architectures with advanced CMOS processes to provide exceptional performance and reliability. To maintain the highest possible performance and reliability of Altera devices, system designers must consider the following operating requirements:

- Operating conditions
- Pin voltage levels
- Output loading
- Power-supply management
- Device programming / erasure

Operating Conditions

When Altera devices are implemented in a system, they are rated according to a set of defined parameters. These parameters are provided in each device family data sheet and include absolute maximum ratings, recommended operating conditions, and DC and AC operating conditions.

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for a particular Altera device. These values are based on experiments conducted with Altera devices, and on theoretical modeling of breakdown and damage mechanisms. These ratings are stress ratings only. The functional operation of Altera devices is not implied at these conditions or at conditions beyond those indicated in the "Recommended Operating Conditions" tables in device family data sheets. For example, I_{OUT} is the absolute current capacity, not the drive capability of an output pin. The output drive characteristics are given as I_{OH} and I_{OL} in the "DC Operating Conditions" table of each device family data sheet.

Device reliability can be impaired if an Altera device operates for extended periods of time at conditions listed in the "Absolute Maximum Ratings" table in each device family data sheet. Operating the device at conditions that exceed these ratings can permanently damage the device.

Recommended Operating Conditions

The functional operation limits for an Altera device, listed in the "Recommended Operating Conditions" table in each device family data sheet, specify limits for all DC and AC parameters. These parameters are expressed differently in other rating sections. For example, the V_{CC} range specified in the "Recommended Operating Conditions" table is the voltage range for safe device operation, while the V_{CC} range specified in the "Absolute Maximum Ratings" table is the power-supply level beyond which the device can be permanently damaged.

DC Operating Conditions

The steady-state voltage and current values expected from Altera devices are provided in the "DC Operating Conditions" table of each device family data sheet. This information includes input voltage sensitivities (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), current drive characteristics (I_{OH} and I_{OL}), and input and output leakage currents (I_I and I_{OZ}).

AC Operating Conditions

The internal and external timing parameters for an Altera device are listed in the "AC Operating Conditions" table in each device family data sheet. These parameters are determined under the conditions specified in the "Recommended Operating Conditions" table. The internal timing parameters are the delays associated with specific architectural features. Device performance can be estimated by following the signal path from a source to the destination and adding the appropriate internal timing parameters. The external timing parameters are specified as pin-to-pin delays when the device is operating under these conditions.

Timing parameters are specified as maximum, minimum, or typical values. A maximum value indicates that the delay will not exceed the specified time. Setup, hold, memory cycle, and pulse width times are expressed as minimum values that the system must provide to ensure reliable device operation. Expected values based on device characteristics are expressed as typical values; actual values can vary.

Pin Voltage Levels

Device pins can be exposed to dangerous voltages during handling or device operation. During handling, pins can be exposed to high-voltage static discharges that cause electrostatic discharge (ESD) damage. During operation, power-supply spikes on the VCC and GND pins or errant logic levels elsewhere in the system can produce logic-level stress with voltages similar to V_{CC} (0 V to 15 V). To minimize these hazards, the user must observe the precautions specified for the following conditions:

- Pin connections
- Latch-up
- Hot-socketing
- ESD

Pin Connections

During project compilation, the MAX+PLUS® II Compiler generates a device utilization report, called a Report File (**.rpt**). The Report File provides information on the pin-outs and connectivity of the device(s) used in the project. The Report File includes a pin-out diagram that shows the user VCCINT, VCCIO, VCC, GNDIO, GNDINT, and GND pins, dedicated function, and unused pins.

The VCCINT, VCCIO, VCC, GNDIO, GNDINT, and GND pins should be tied to the V_{CC} or ground planes, respectively, on the printed circuit board (PCB). Dedicated input pins used in a design and I/O pins configured as inputs should always be driven by an active source. I/O pins configured as bidirectional pins should always be driven whenever the I/O pin is used as an input. Unused dedicated input and I/O pins are marked in the Report File as GND and RESERVED, respectively. Unused dedicated inputs should be tied to the ground plane. Otherwise, these pins may “float” in an indeterminate state, possibly increasing DC current in the device and introducing noise into the system. To prevent unused I/O pins from floating, they are driven by an internal signal and are reported as RESERVED. All RESERVED I/O pins should remain unconnected. Tying a RESERVED I/O pin to V_{CC}, ground, or another signal source can create contention that can damage the output driver on the device.

Some Altera devices include the MultiVolt™ feature, in which devices can interface to multiple voltage systems. These devices may have separate VCCIO (I/O power) and VCCINT (internal power) pins. Refer to the device data sheets for limits on V_{CCIO} and V_{CCINT} voltage ranges.

For proper operation, signals on the input and output pins must be in the following range:

$$\text{Ground} \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CCINT}$$

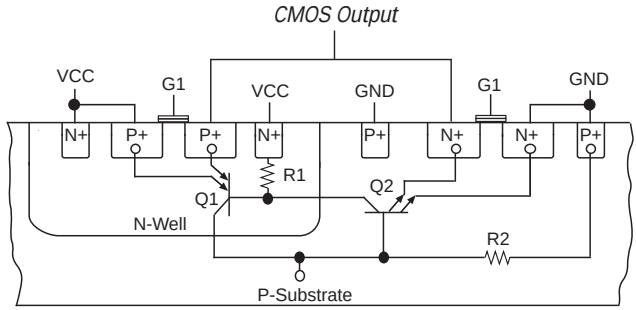
Some 3.3-V devices can accept V_{IN} that is greater than V_{CCINT}. Refer to the device data sheets for specific voltage limitations.

If a design connects GNDINT and GNDIO to different ground planes, GNDINT and GNDIO must always be within 1.0 V. Otherwise, incorrect device operation may occur.

Latch-Up

Parasitic bipolar transistors, which are present in the fundamental structure of CMOS devices, can create paths in the device for destructive currents. Typically, the base-emitter and base-collector junctions of these parasitic transistors are not forward-biased, so they are not turned on. Figure 1 shows a cross-section of a CMOS wafer and primary parasitic transistors (labeled Q1 and Q2). To ensure that all junctions remain reverse-biased, the P-type substrate is connected to the most negative voltage available on the device (ground), and the N-type well structure is connected to the most positive voltage on the device (V_{CC}). Figure 1 also shows the parasitic resistors (labeled R1 and R2) that occur in the CMOS structure.

Figure 1. Parasitic Bipolar Transistors in CMOS Devices



Catastrophic failure can occur if these parasitic structures begin to conduct, because the effect is regenerative and reinforces itself until potentially destructive currents are produced. The two parasitic transistors combine to form a silicon-controlled rectified (SCR). The latch-up effect occurs when the SCR is turned on, resulting in high current flow through the CMOS device.

The SCR can be turned on by transients occurring on the gates of the CMOS device or on the output of the CMOS device. Because I/O pins are connected to the input and output buffers, latch-up can occur on either buffer.

If the I/O pad is driven above V_{CCINT} or below ground, latch-up may occur. (Most 3.3-V devices, such as those from the FLEX® 10KA and MAX® 7000A device families, are designed to withstand input voltages above V_{CCINT}; however, there is a level at which the device may be damaged. Refer to the device data sheets for specifications.) When the output pad is driven below ground, Q2 will turn on as its emitter becomes more negative than its base. This effect causes Q1 to turn on as its base becomes more negative than its collector. The current flow through Q1 causes Q2's base to become more positive (due to the voltage drop over parasitic resistor R2). The current flow through Q2 causes Q1's base to become more negative (due to the voltage drop over parasitic resistor R1). Both current flows cause Q1 and Q2 to conduct more current, in a regenerative effect. As the current flows through the parasitic transistors, the voltage drops through the increase in the resistor. Once started, the cycle will continue until the device is powered down or damaged by high current flow.

When the input buffer pad is driven below ground, current is injected into the substrate via the diffused ESD protection resistor (see "Electrostatic Discharge" on page 491). This current can raise the voltage level of the base of Q2, starting the latch-up cycle. Again, the cycle will continue until the device is powered down or damaged by high current flow.

Conversely, if the I/O pad is driven above V_{CC}, Q1 will turn on as its emitter is driven higher than its base. The same regenerative effect occurs as in the undershoot case.

The I/O pad may be driven outside of V_{CC} and ground due to signal ringing, undershoot, or overshoot. The board should be designed to minimize these effects and therefore to prevent latch-up.

Altera devices have been designed to minimize the effects of latch-up that is caused by power-supply and I/O pin transients. Under recommended operating conditions, all devices can withstand input voltage extremes between ground – 1 V and V_{CCINT} + 1 V, as well as input currents of 100 mA or less that are forced through the device pins.

To minimize the chances of inducing latch-up during power-up, ground should be applied to the device first, then V_{CCINT} and V_{CCIO}, and finally the inputs. The power should be removed from the device in the reverse order: the inputs are removed first, then V_{CCINT} and V_{CCIO}, and finally ground. Inputs of some devices may be driven before powering V_{CCINT} and V_{CCIO}. Consult the individual device data sheets.

Simultaneous application of inputs and V_{CCINT} and V_{CCIO} to the device, which can occur as the power supply rises during power-up, should be safe as long as V_{CCINT} and V_{CCIO} meet the maximum rise time. The designer should ensure that the inputs cannot rise faster than the supply at the VCCINT and VCCIO pins.

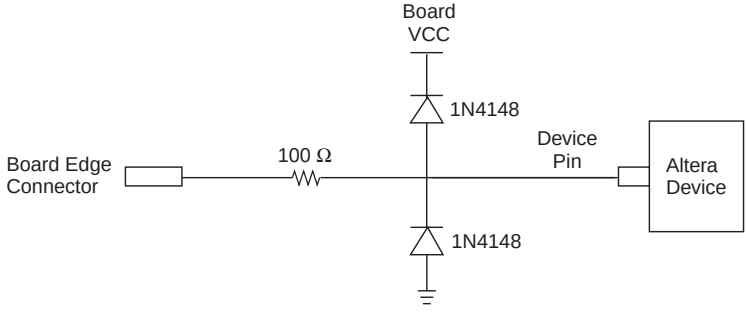
Hot-Socketing

Latch-up frequently occurs when electrical subsystems are "hot-socketed" or plugged into active hardware. When a subsystem is hot-socketed, the logic levels often appear at the subsystem's logic devices before the power supply can provide current to the V_{CC} and ground grid of the subsystem board. This condition can lead to latch-up.

Increasing the length of the V_{CC} and ground connections can reduce the chances of latch-up during hot-socketing. If metal "fingers" are used for the board connection, the V_{CC} and ground fingers at the card edge should be longer than the logic connections. The difference in length will cause the power supply to appear at the device before the logic levels, which is usually sufficient to prevent latch-up. Off-the-shelf connectors with longer V_{CC} and ground connections can provide similar results.

Implementing the circuitry shown in Figure 2 also provides protection against latch-up during hot-socketing. The diode structure provides a "clamp" level on the input voltage, preventing it from swinging more than one diode-drop away from a power rail (–0.7 V to V_{CC} + 0.7 V). The series resistor also reduces the possibility of latch-up by restricting the current to the device input and clamp diodes. This circuitry provides the maximum protection against latch-up, but is usually required only if the input on the device is tied directly to the edge connector. Device inputs that are driven by other circuit elements in the subsystem are generally safe from latch-up, because these elements provide a natural delay before the logic levels are established.

Figure 2. Hot-Socket Protection



Electrostatic Discharge

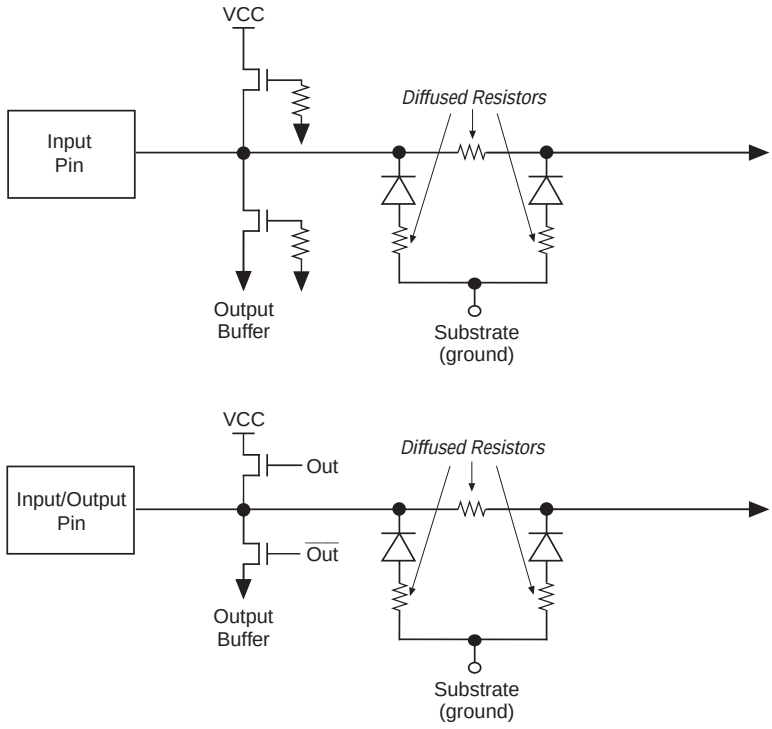
Electrostatic discharge (ESD) resulting from improper device handling can cause device failure that may manifest itself in the following ways:

- Immediate functional failure
- Degraded I/O performance
- Decreased long-term reliability

Handling devices during the programming cycle increases exposure to potential static-induced failure. Synthetic materials used in clothing can store large amounts of static electricity, which can cause ESD. During normal activity, the human body can generate voltages of up to tens of kilovolts (kV). Therefore, to reduce the likelihood of ESD damage, users should wear ground straps when handling devices and ground all surfaces that contact devices.

Altera devices include special structures that reduce the effects of ESD on the pins. Figure 3 shows a typical input structure for an Altera device. Diode structures and an output buffer shunt harmful voltages to ground before the circuitry can be damaged. Most Altera devices can withstand ESD voltages greater than 2 kV, but all devices can withstand ESD voltages up to 1 kV. ESD performance data is reported in Altera's reliability reports.

Figure 3. Altera Device Input Protection Structures



Output Loading

Output loading is typically resistive and / or capacitive. During development, the designer should ensure that the target device can supply both the current and speed necessary for the loads.

Resistive Loading

Resistive loading exists whenever a device output sinks or sources a current in a steady state (e.g., devices with TTL inputs, terminated buses, and discrete bipolar transistors).

Output drive characteristics (I_{OH} and I_{OL}), which are functions of output voltages (V_{OH} and V_{OL}), are listed in each device family data sheet. Under DC conditions, the output current capabilities determine the minimum resistance of a load while still maintaining the necessary output voltage. If the system requires higher currents, such as those necessary to drive an LED or a relay, a high-current buffer or a discrete current switch must be used.

Short-circuit conditions—where I_{OH} and I_{OL} exceed the absolute maximum rating (I_{OUT})—can permanently damage the device.

Capacitive Loading

The "AC Operating Conditions" table in each device family data sheet specifies an output capacitance condition (C1) for parameters relating to external performance. For most Altera devices, C1 is 35 pF for active signals and 5 pF for disabling output buffers.

Device packages and board-level trace capacitance contribute the majority of loading capacitance. The specified 35-pF load condition is a representative value for most CMOS circuits. For applications in which a device drives a higher capacitance, performance decreases as the capacitive load increases.

Device sockets are a source of both capacitive and inductive loading. Once a system is finalized for production, sockets should be removed if possible, and the devices should be mounted directly onto the PCB. Direct board mounting reduces both the capacitive and inductive loads as well as noise from socket contacts.

To ensure the highest circuit performance, the capacitance on device outputs should be minimized. Because wiring traces on the PCB, device input pins, and device packaging all contribute to the total capacitance, the following guidelines should be observed:

- Board layout should ensure that signals run perpendicular to each other to provide a minimum capacitive coupling effect. Also, signal traces should be kept as short as possible.
- A high-current buffer should be used to speed the signal to all destinations for networks in which a single source drives many loads.

The lack of V_{CC} and ground planes or excessive trace lengths can cause problems with radiated coupling of noise into logic signals and transmission-line effects on signal quality. These ringing and noise elements on logic levels can lead to circuit reliability problems. When recommended layout practices cannot be implemented to prevent transmission-line problems, a small series resistor (10 Ω to 30 Ω) can be used to reduce the undershoot or overshoot magnitude on signal edges. This resistor dampens the ringing that can occur on long board traces and prevents false triggering.

For more information, see *Application Note 75 (High-Speed Board Designs)* in this data book.

Power-Supply Management

Although Altera devices are designed to minimize noise generation and susceptibility, they can be sensitive to fluctuations in power supply and input lines, like all CMOS devices.

To minimize the effect of these fluctuations, the system designer must pay special attention to the following factors:

- V_{CC} and ground planes
- Decoupling capacitors
- V_{CC} rise time
- Current dissipation

VCC & Ground Planes

The system designer can minimize power-supply noise or "ground bounce" by providing separate V_{CC} and ground planes for every PCB, thus ensuring a large current-sink capability, noise protection, and shielding for logic signals on the board. If an entire plane cannot be provided, the widest possible ground and V_{CC} traces should be created throughout the entire board. Logic-width traces should not be used to carry the power supply. Although V_{CC} and ground planes tend to increase the capacitive load of the traces, they significantly reduce system noise and dramatically increase system reliability.

Decoupling Capacitors

Each VCC and GND pin should be connected directly to the V_{CC} and ground planes in the PCB. Decoupling requirements are based on the amount of logic used in the device and the output switching requirements. As the number of I/O pins and the capacitive load on the pins increase, more decoupling capacitance is required. Each pair of VCC and GND pins should be decoupled with a 0.2-µF power-supply decoupling capacitor, located as close as possible to the Altera device. When using a device with separate VCCINT and VCCIO pins, each VCCIO/GNDIO and VCCINT/GNDINT pair should be decoupled with a 0.2-µF capacitor. Devices with separate VCCINT and VCCIO pins, but not separate GNDIO and GNDINT pins, should be decoupled with capacitors from V_{CCIO} and V_{CCINT} to ground. For less dense designs, a reduction in the number of capacitors may be acceptable. Decoupling capacitors should have a good frequency response, such as monolithic-ceramic capacitors.

Each PCB should also have a large-capacity, general-purpose, electrolytic capacitor network to stabilize the power supply. A 100-µF capacitor should be placed immediately adjacent to the location where the power-supply lines come into the PCB. If a transformer or regulator is used to change the voltage level, the capacitor should be placed immediately after the final stage that develops the device's power supply. This capacitor provides a beneficial leveling effect that supplies extra current when a large number of nodes switch simultaneously in a circuit. However, the larger the power supply capacitor, the longer the time required to bring the maximum V_{CC} to the operating level. The size of the capacitor must not force the V_{CC} rise time to violate the maximum rise time.

V_{CC} Rise Time

When power is applied to an Altera device, the device initiates a Power-On Reset (POR) event, typically as V_{CC} approaches 1.5 V to 2.0 V. The POR event occurs only if V_{CC} reaches the recommended operating range within a certain period of time (specified as a maximum V_{CC} rise time). Slower rise times can cause incorrect device initialization and functional failure. The maximum V_{CC} rise times for Altera devices are provided in the "Recommended Operating Conditions" section of each device family data sheet.

The POR time is the time required after V_{CC} reaches the recommended operating range to clear device registers, configure I/O pins, and release tri-states. Once this initialization is complete, the device is ready to begin logic operation. The POR time does not exceed 100 ms.

Current Dissipation

Each Altera device is designed to consume a minimal amount of power while providing high performance. Because these two design goals can conflict, Altera devices and software tools allow designers to monitor and control the current with built-in device features.

Each MAX 9000 and MAX 7000 device macrocell can be configured for either high performance or low power consumption during design entry. Turning on the macrocell's Turbo Bit™ allows the macrocell to function in a high-performance mode at the specified device ratings. If the Turbo Bit is turned off, the macrocell's built-in power-saving mode trades higher performance for lower current consumption.

MAX 9000 and MAX 7000 devices operating in low-power mode consume less current. The supply current (I_{CC}) can be reduced by approximately 50%, depending on the design and operating frequency. I_{CC} vs. frequency graphs are provided in the *MAX 9000 Programmable Logic Device Family*, and *MAX 7000 Programmable Logic Device Family* data sheets. For a device with the Turbo Bit option, the graph provides two curves: one showing I_{CC} versus frequency when all macrocells have their Turbo Bits turned on, and the other with all Turbo Bits off. Because most designs use a combination of turbo and non-turbo macrocells, a formula that accounts for this ratio and the frequency of operation is also provided with the graph. The values shown in the graph and formula are measured with no output loads and represent only the current consumed by device operation.

Many Classic devices also have a Turbo Bit option. A Classic device operating in low-power mode enters a standby mode after 100 ns of inactivity (i.e., when no inputs or outputs have changed). An input signal transition "wakes" the device, which then performs normally until the next standby mode period. However, the input signal incurs an additional delay—specified as the non-turbo delay adder in device family data sheets—as it wakes and propagates through the device.

Device Programming/ Erasure

MAX 9000, MAX 7000, MAX 5000, Classic™, and Configuration EPROM devices use non-volatile, reprogrammable EPROM or EEPROM memory elements to retain configuration data. Therefore, configuration data does not need to be reloaded when the system powers up. EPROM and EEPROM memory elements share similar programming characteristics, but different erasure mechanisms.

All Altera EEPROM-based devices are reprogrammable. EEPROM elements are electrically erasable and therefore do not have an erasure window. EEPROM-based devices are automatically erased immediately before being programmed, and can be reprogrammed at least 100 times. Most devices can be reliably reprogrammed many more times beyond this specified minimum. During programming, the EEPROM cell does not require a special VPP pin with a higher programming voltage. The device internally generates the required voltage.

Altera's EPROM-based devices are available in both plastic and ceramic packages. EPROM devices in plastic packages are one-time-programmable (OTP) devices; windowed ceramic packages allow erasure by exposure to UV light. Altera EPROM-based devices begin to erase when exposed to lights with wavelengths shorter than 4,000 Å. Because fluorescent lighting and sunlight fall into this range, an opaque label must be placed over the device window to ensure long-term reliability. To completely erase a device, it must be exposed to UV light with a wavelength of 2,540 Å. Devices should be erased for one hour by an eraser system with a power rating of 12,000 $\mu W / cm^2$. Altera devices can be damaged by long-term exposure to high-intensity UV light.

Altera EPROM-based devices can be programmed and erased at least 25 times, provided that the recommended erasure exposure levels are followed. However, most devices can be reliably erased and reprogrammed many more times beyond this specified minimum.